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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,823	03/31/2004	Franck Roche	00RO30654423	5289

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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,823	ROCHE ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/30/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear after examining the specification what the applicant means by "gathering", so it has been interpreted for the remainder of this office action to simply be a collection of instructions capable of addressing the extended address area, while the first group comprises instructions which can only access a lower memory area. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 5-9, 11-12, 15-19, 21-22, and 25-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Baum et al. (USPN 5,423,013, herein Baum).

6. As per Claim 1, Baum teaches: A microprocessor comprising:

a processing unit (Column 1, Line 8);

a memory connected to said processing unit and comprising an addressable memory space for a lower memory area and an extended memory area (Column 1, Line 54 – Column 2 Line 1);

means for connecting to and accessing said addressable memory space (Figure 7, ERA. See Column 12, Lines 30-31);

means for executing an instruction set for accessing said addressable memory space, the instruction set comprising a first instruction group for accessing said lower memory area (Column 3, Line 67 – Column 4, Line 1), and a second instruction group distinct from the first instruction group for gathering instructions in the instruction set for accessing said extended memory area (Column 3, Line 67 – Column 4, Line 3); and

means for preventing access to said extended memory area when executing the first instruction group (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

7. As per Claim 2, Baum teaches: A microprocessor according to claim 1, wherein each location in said addressable memory space is associated with a respective access address; and further comprising means for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing the first instruction group (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

8. As per Claim 5, Baum teaches: A microprocessor according to claim 1, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area (Column 14, Lines 53-56); and further comprising means for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

9. As per Claim 6, Baum teaches: A microprocessor according to claim 1, wherein the second instruction group comprises instructions for accessing said extended memory area (Column 3, Line 67 – Column 4, Line 5) in an indirect addressing mode (Column 14, Lines 53-56).

10. As per Claim 7, Baum teaches: A microprocessor according to claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

11. As per Claim 8, Baum teaches: A microprocessor according to claim 6, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area (Column 3, Line 67 – Column 4, Line 5).

12. As per Claim 9, Baum teaches: A microprocessor according to claim 1, wherein said means for connecting to and accessing said addressable memory space comprises an address bus (Figure 7, ERA. See Column 12, Lines 30-31); and further comprising a program pointer register having a size corresponding to a size of said address bus for enabling access to a program instruction to be executed that is located at an arbitrary location in said addressable memory space (Column 13, Lines 30-31).

13. As per Claim 11, Baum teaches: A microprocessor comprising:

a processing unit (Column 1, Line 8);

a memory connected to said processing unit and comprising an addressable memory space for a lower memory area and an extended memory area (Column 1, Line 54 – Column 2, Line 1);

an address bus connected to said memory (Figure 7, ERA. See Column 12, Lines 30-31); and

an instruction set for accessing said addressable memory space, the instruction set comprising

a first instruction group for accessing said lower memory area (Column 3, Line 67 – Column 4, Line 1),

a second instruction group distinct from the first instruction group for gathering instructions in the instruction set for accessing said extended memory area (Column 3, Line 67 – Column 4, Line 3), and

instructions for preventing access to said extended memory area when executing the first instruction group (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

14. As per Claim 12, Baum teaches: A microprocessor according to claim 11, wherein each location in said addressable memory space is associated with a respective access address; and wherein said instruction set further comprises instructions for forcing an access address of a location to be accessed to point to a location in said lower memory area when executing the first instruction group (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

15. As per Claim 15, Baum teaches: A microprocessor according to claim 11, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in said lower memory area (Column 14, Lines 53-56); and wherein said instruction set further comprises instructions for forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in said lower memory area and points to this area (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

16. As per Claim 16, Baum teaches: A microprocessor according to claim 11, wherein the second instruction group comprises instructions for accessing said extended memory area (Column 3, Line 67 – Column 4, Line 5) in an indirect

addressing mode (Column 14, Lines 53-56).

17. As per Claim 17, Baum teaches: A microprocessor according to claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located in said lower memory area (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

18. As per Claim 18, Baum teaches: A microprocessor according to claim 16, wherein in the indirect addressing mode of said extended memory area, pointers that determine an address of a memory location to be accessed are located within said extended memory area (Column 3, Line 67 – Column 4, Line 5).

19. As per Claim 19, Baum teaches: A microprocessor according to claim 11, further comprising a program pointer register having a size corresponding to a size of said address bus (Figure 7, ERA. See Column 13, Lines 30-31) for enabling access to a program instruction to be executed that is located at an arbitrary location in said addressable memory space (Column 3, Line 67 – Column 4, Line 5).

20. As per Claim 21, Baum teaches: A method for accessing a memory used by a microprocessor, the microprocessor comprising a processing unit (Column 1, Line 8), an address bus connected to the processing unit (Figure 7, ERA. See Column 12, Lines 30-31), with the memory being connected to the address bus and comprising an

addressable memory space for a lower memory area and an extended memory area, the method comprising (Column 1 Lines 16-19):

accessing the lower memory area using a first instruction group (Column 3, Line 67 – Column 4, Line 1);

gathering instructions in the instruction set for accessing the extended memory area (Column 3, Line 67 – Column 4, Line 3); and

preventing access to the extended memory area when executing the first instruction group (Column 3, Line 67 – Column 4, Line 5).

21. As per Claim 22, Baum teaches: A method according to claim 21, wherein each location in the addressable memory space is associated with a respective access address; and further comprising instructions for forcing an access address of a location to be accessed to point to a location in the lower memory area when executing the first instruction group (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

22. As per Claim 25, Baum teaches: A method according to claim 21, wherein the first instruction group comprises indirect mode addressing instructions for accessing a location in the lower memory area (Column 14, Lines 53-56); and further comprising forcing an address and a value of a pointer that specifies access in the indirect mode so that the pointer is located in the lower memory area and points to this area (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

23. As per Claim 26, Baum teaches: A method according to claim 21, wherein the second instruction group comprises instructions for accessing the extended memory area (Column 3, Line 67 – Column 4, Line 5) in an indirect addressing mode (Column 14, Lines 53-56).

24. As per Claim 27, Baum teaches: A method according to claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located in the lower memory area (Column 3, Line 67 – Column 4, Line 5, and Column 7, Lines 12-21).

25. As per Claim 28, Baum teaches: A method according to claim 26, wherein in the indirect addressing mode of the extended memory area, pointers that determine an address of a memory location to be accessed are located within the extended memory area (Column 3, Line 67 – Column 4, Line 5).

26. As per Claim 29, Baum teaches: A method according to claim 21, wherein the microprocessor further comprises a program pointer register having a size corresponding to a size of the address bus (Figure 7, ERA. See Column 13, Lines 30-31) for enabling access to a program instruction to be executed that is located at an arbitrary location in the addressable memory space (Column 3, Line 67 – Column 4, Line 5).

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 3-4, 13-14, and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baum, in view of Suleman.

29. As per Claim 3, Baum teaches: A microprocessor according to claim 1, further comprising at least one internal register (Examiner is taking official notice that a register file, and thus internal registers, are in almost every processing machine that executes instructions and operates a memory, and would have been in the system intended for Baum's invention), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said addressable memory space; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

Baum teaches a system to address a very large memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an

instruction set to run instructions, one of ordinary skill in the art would have recognized that if Baum's invention was to be implemented in an 8086 machine in order to take advantage of the increased memory addressing size, then they would have Jump, Call, and Move instructions available to them.

30. As per Claim 4, Baum teaches: A microprocessor according to claim 1, wherein each location in said addressable memory space is associated with a respective access address (Column 1, Line 67 – Column 2, Line 12); and

means for maintaining an address of a jump destination location so that it points to a location in said lower memory area (Column 3, Line 67 – Column 4, Line 5), but fails to teach:

for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area.

Baum teaches a system to address a very large memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Baum's invention was to be implemented in an 8086 machine in order to take advantage of the increased memory addressing size, then they would have Jump, Call, and Move instructions available to them.

31. As per Claim 13, Baum teaches: A microprocessor according to claim 11, further comprising at least one internal register (Examiner is taking official notice that a register file, and thus internal registers, are in almost every processing machine that executes instructions and operates a memory, and would have been in the system intended for Baum's invention), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in said addressable memory space; and

data transfer instructions between the arbitrary memory location and said at least one internal register.

Baum teaches a system to address a very large memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Baum's invention was to be implemented in an 8086 machine in order to take advantage of the increased memory addressing size, then they would have Jump, Call, and Move instructions available to them.

14. A microprocessor according to claim 11, wherein each location in said addressable memory space is associated with a respective access address (Column 1, Line 67 – Column 2, Line 12); and

said instruction set further comprises instructions for maintaining an address of a jump destination location so that it points to a location in said lower memory area (Column 3, Line 67 – Column 4, Line 5, but fails to teach:

executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in said lower memory area.

Baum teaches a system to address a very large memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Baum's invention was to be implemented in an 8086 machine in order to take advantage of the increased memory addressing size, then they would have Jump, Call, and Move instructions available to them.

32. As per Claim 23, Baum teaches: A method according to claim 21, further comprising at least one internal register (Examiner is taking official notice that a register file, and thus internal registers, are in almost every processing machine that executes instructions and operates a memory, and would have been in the system intended for Baum's invention), but fails to teach:

wherein the second instruction group comprises:

jump and routine call instructions at an arbitrary memory location in the addressable memory space; and

data transfer instructions between the arbitrary memory location and the at least one internal register.

Baum teaches a system to address a very large memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an instruction set to run instructions, one of ordinary skill in the art would have recognized that if Baum's invention was to be implemented in an 8086 machine in order to take advantage of the increased memory addressing size, then they would have Jump, Call, and Move instructions available to them.

33. As per Claim 24, Baum teaches: A method according to claim 21, wherein each location in the addressable memory space is associated with a respective access address (Column 1, Line 67 – Column 2, Line 12); and further comprising maintaining an address of a jump destination location so that it points to a location in the lower memory area (Column 3, Line 67 – Column 4, Line 5), but fails to teach:

for executing jump or routine call instructions from the first instruction group in a direct addressing mode from a location in the lower memory area.

Baum teaches a system to address a very large memory, but does not specifically disclose the instructions the system is capable of performing. However, Suleman teaches that in the Intel 8086 architecture, Jump (Page 14), Call (Page 16), and Move (Page 2) instructions are provided. Given that a computer needs an

instruction set to run instructions, one of ordinary skill in the art would have recognized that if Baum's invention was to be implemented in an 8086 machine in order to take advantage of the increased memory addressing size, then they would have Jump, Call, and Move instructions available to them.

34. Claims 10, 20, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baum.

35. As per Claims 10, 20, and 30, with Claim 10 being exemplary, Baum teaches a microprocessor according to claim 1, but fails to teach:

wherein said lower memory area is accessible over 16 bits and said extended memory area is accessible over 24 bits.

Baum teaches a method to extend register addressing, from a smaller bit size to a larger one, and in his specific case, 24 or 32 bits to a larger size. However, one of ordinary skill in the art would have recognized that the idea behind allowing systems of smaller bit size to operate on larger memories could be applied to any memory size, regardless of not being the exact sizes disclosed by Baum. In addition, changing bit size is not considered to be a patentable distinction. See *In re Rose,* 200 F.2d 459, 463, 105 USPQ 237, 240 (CCPA 1955). Claims 20 and 30 teach similar limitations and are rejected for the same reason.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

37. Gong (USPN 6,192,476) teaches a method of controlling access to a resource by setting permissions, which allow certain instructions to access only certain parts of the memory.

38. Abrams (United States Patent Application Publication 2003/0204745) teaches a method to prevent buffer overflows by not allowing instructions to modify a specific area of memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert E Fennema
Examiner
Art Unit 2183

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